Homework 4: Sequential Chips

Objective:

Build all gates described in Chapter 3 (see table below), which will test your understanding of sequential chips for our HACK architecture.

Grading method:

If the chip passes *all* the tests specified in the supplied test script, it receives 60% of the grade. 30% goes to it being well built (the lowest number of chips to implement), with the remaining 10% going towards documentation provided for each chip. Generally speaking, we prefer implementations that *use as few chip **parts** as possible,* even if it implies a less efficient chip design (in term of # of AND/OR/NOT chips). Higher-level chips are considered as one chip part (ex. Mux, DMux, Or8Way, etc.)

What do you turn in?

A Word document (or PDF) with screen shots of each of the working (or not) logic gates. You should also upload the documentation.pdf file (see Documentation Instructions for guidelines on how to do this) per Project Submission Guidelines.

Chip + Test	***Working?***	***Well built?***
Bit	/ 7	/ 3
Register	/ 7	/ 3
RAM8	/ 7	/ 3
RAM64	/ 7	/ 3
RAM512	/ 7	/ 3
RAM4K	/ 7	/ 3
RAM16K	/ 7	/ 3
PC	/ 11	/ 9
Subtotal	/ 60	/ 30
Documentation	/ 10	

See http://nand2tetris.org/03.php for some tips/resources/tools (note that the assignment on the website may be substantially different from the assignment that is described above, if you need clarification email your instructor. You will be graded based on this documents requirements).